Separating a wafer into chips using dry etching and backside grinding

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This short articles describes a method to separate a wafer into photonic chips or dice, using dry etching and backside grinding. This method enables smooth chip facets that are advantageous for edge coupling with fibers or other chips.

Keywords: Dry etching, grinding, chip release

To separate a full wafer into small chips or dice ("chip release"), one can often use dicing. However, dicing often leads to rough chip facets that have challenges in edge coupling with fibers or other chips. Here, a scheme to separate a wafer into chips using dry etching and backside grinding is shown. This process has been used in our standard fabrication of silicon nitride photonic chips. The process flow for chip release is shown in Fig. 1. The key method used here is deep reactive ion etching (RIE) to etch the wafer frontside (in our case, mainly SiO_2 and Si), which defines the chip facet, and then backside grinding to separate the chips. The key advantage of this method is the ability to achieve much smoother chip facets compared with the facets made by the normal dicing method. In addition, the deep RIE can work with chip separation distance smaller than 10 μm, while dicing typically requires a distance larger than 100 μm. Thus chips can be placed more tightly on the wafer.

Figure 2 shows the SEM image of the chip facet with superior quality, using deep RIE to define the facet. A vertical and smooth facet is critical for edge coupling (see examples in ref. [1–3], where the Si_3N_4 chips are directly edge-coupled to laser diodes or DFB lasers). In these cases, the smooth facet of the Si_3N_4 chips allows for seamless contact with the laser diodes, thus attaining high optical power coupling efficiency from the lasers to the Si_3N_4 chips.

More details of the fabrication process flow are shown below.

Photolithography: The lithography step is to define the chip boundaries and facets. Photolithography can be implemented using either a direct laser writer, or a contact mask aligner. Both lithography tools use UV light source e.g. from mercury i-line, and require alignment as the chip release layer needs to be superimposed on the waveguide pattern with reasonable overlap precision. Both processes can reach a minimum feature size of 1 μm (determined by the UV wavelength, photoresist thickness, and exposure parameters). To reach the optimal lithography quality, optimal parameter sets of dose and focus are needed, and can be found via a series of tests. Both methods require alignment markers for lithography alignment.

As an example, Fig. 3 shows the design layout to separate a 4-inch wafer into chips, with four alignment markers (cross) used to align the chip release layer to the waveguide pattern.

As deep RIE follows, the photoresist needs to be thick enough, and the deep RIE needs to have a high SiO_2-to-resist and Si-to-resist selectivity. In addition, deep RIE requires a long etch time, thus the wafer backside needs to be thoroughly cleaned such that resist burning during etching does not happen. With several concerns and limitations, currently we can use two photoresists (available in EPFL CMi) in the chip release lithography: AZ 9260 and AZ 10XT-60. Both resists are DNQ-based *positive* photoresists with high viscosity, thus they can form thick resist masks from 5 μm to 20 μm thickness. They are UV-sensitive, thus can be exposed by mercury i-line and h-line from 310 to 410 nm wavelength. In the chip release process, a resist mask of 8 – 10 μm thickness is coated on the wafer after an HMDS layer is applied as an adhesion promoter on the heated wafer substrate. After the resist coating, the wafer is placed in a humid environment for 20 min, in order to rehydrate the photoresist. This is because that both resists are based on DNQ, and the photo-chemical reaction of DNQ consumes water and releases nitrogen. The resist rehydration is required in order to achieve complete photo-chemical reaction, and removal of exposed resist after resist development.

After the rehydration of the photoresist, the wafer is exposed with UV lithography described above. After the exposure, the resist is developed. An examination of exposure / development results with an optical microscope is needed. Figure 4 compares the microscope images of chip boundaries after photoresist development. The bad lithography quality can be a result from insufficient exposure (usually due to insufficient dose), insufficient development, or edge bead removal (EBR) issues.

Before the deep RIE, two steps need to be performed: 1. As mentioned earlier, the photo-chemical reaction of DNQ consumes water and releases nitrogen. RIE generates plasma and can emit UV light, which would expose the unexposed resist. The release of nitrogen can swell the resist, leading to critical dimension (CD) drift and a rough resist surface. Thus, to prevent the resist exposure by the UV light during deep RIE, a flood exposure with sufficient dose is needed. 2. The wafer needs a thorough SRD cleaning, in order to remove backside contamination during resist development. Once the chip release pattern

is well defined on the resist, the wafer can proceed with deep RIE.

Deep RIE: For the deep RIE of SiO_2, the ideal process needs to be: 1. Fast (i. e. high etch rate); 2. High selectivity of SiO_2 to photoresist; 3. Vertical; 4. Smooth. Including all factors together and their balance, our dry etching process has an etch rate of around 340 nm/min using the CMi standard process "SiO_2 PR 3:1", and the actual SiO_2-to-resist selectivity is 4. Typically, for 7 μm SiO_2, an etch time of 25 min is needed.

It is then followed by deep RIE of Si. The chosen process recipe for Si etch is a **Bosch process**, and has an etch rate of Si around 5 μm/min, and a Si-to-resist selectivity that exceeds 75. Typically, an etch time of 45 min removes more than 250 μm Si depth with the Bosch process.

Grinding: The last step is the grinding of the wafer backside. If the wafer backside has SiO_2, the SiO_2 needs to be removed before the grinding of Si. The grinder should be configured for Si grinding. The wafer frontside needs to be taped before the grinding. The final sample thickness is 250 μm (chip thickness) + 140 μm (tape thickness) = 390 μm. The thickness control needs to be reasonably precise, so the polishing rate has to be calibrated in the first run (e.g. to a thickness value around 500 μm).

To start the grinding, first of all, make sure that the adequate wheel is installed on the tool . Run a first grinding with a target thickness of 500 μm (360 μm wafer thickness +140 μm tape thickness). Check the final thickness and adjust it with the offset parameter on the tool. All subsequent wafers can be ground in one step to the final thickness of 390 μm (250 μm wafer thickness +140 μm tape thickness). After the grinding is complete, the tape needs to be fully cured (two or three passes under the UV lamp), before being cut and stored in a box for collection. Then the chips can be easily detached from the tape.

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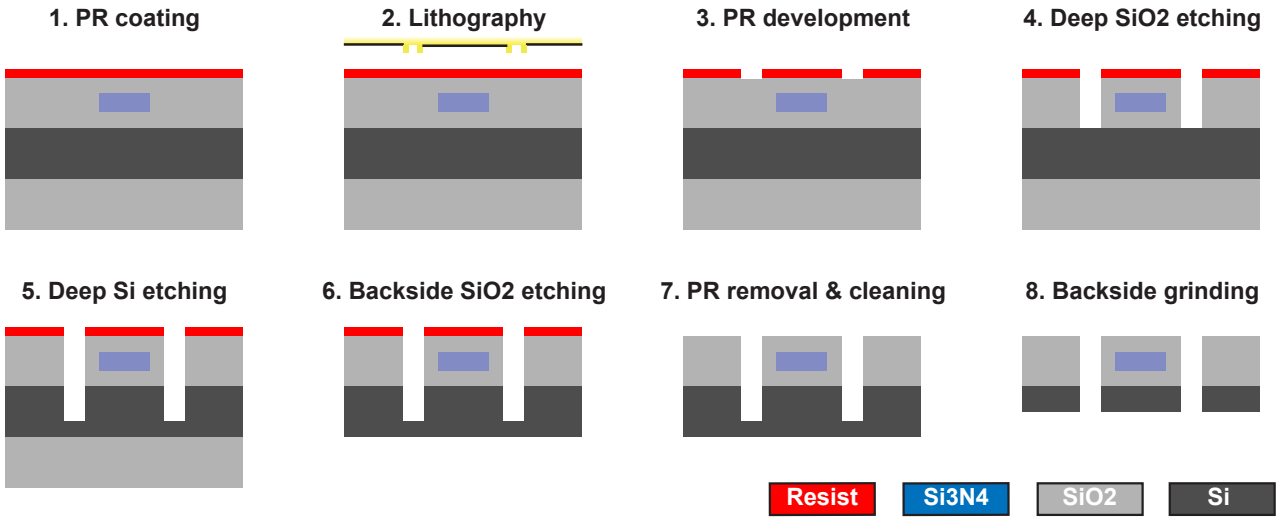

FIG. 1. Simplified process flow of chip release.

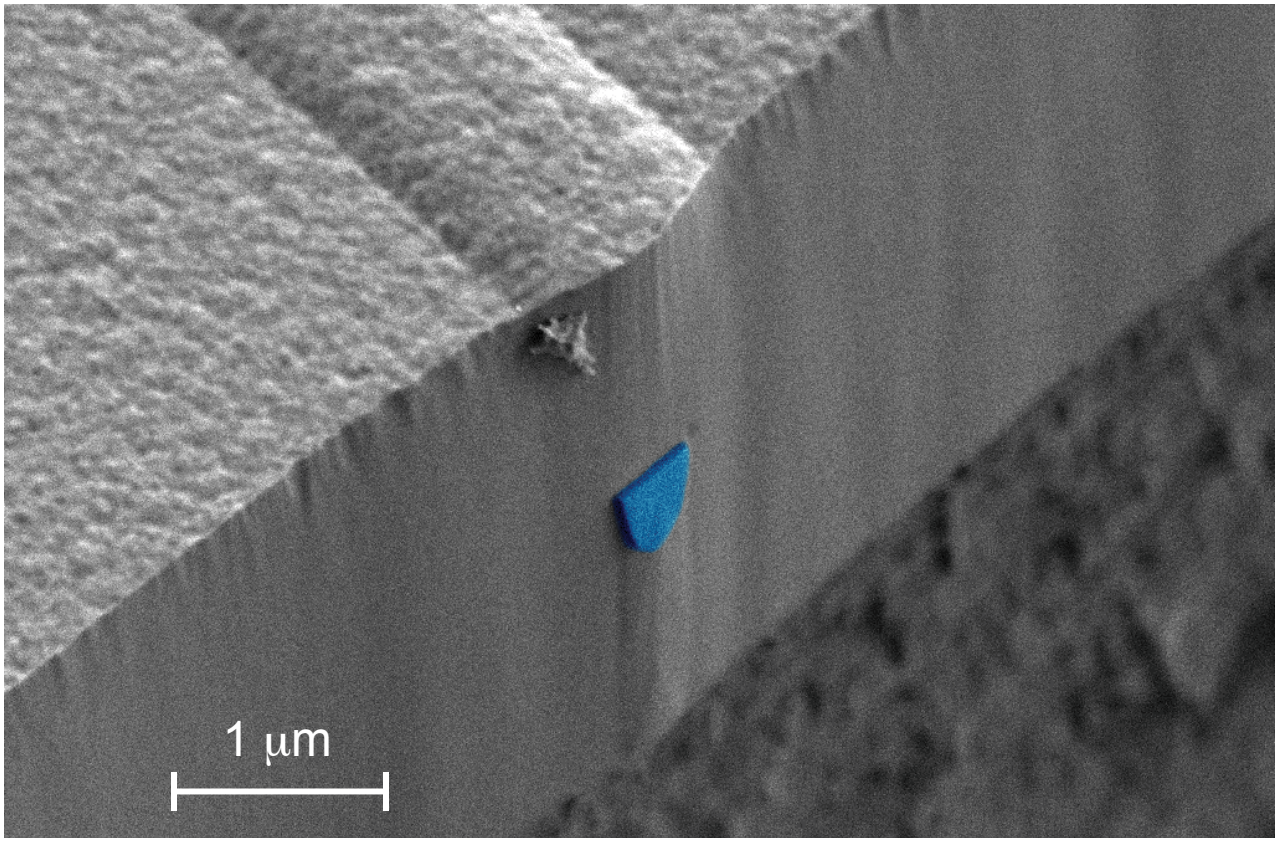

FIG. 2. SEM image showing the chip facet with superior quality, using deep RIE of SiO_2 to define the facet. Silicon nitride waveguide taper, fully buried in SiO_2, is blue-coloured.

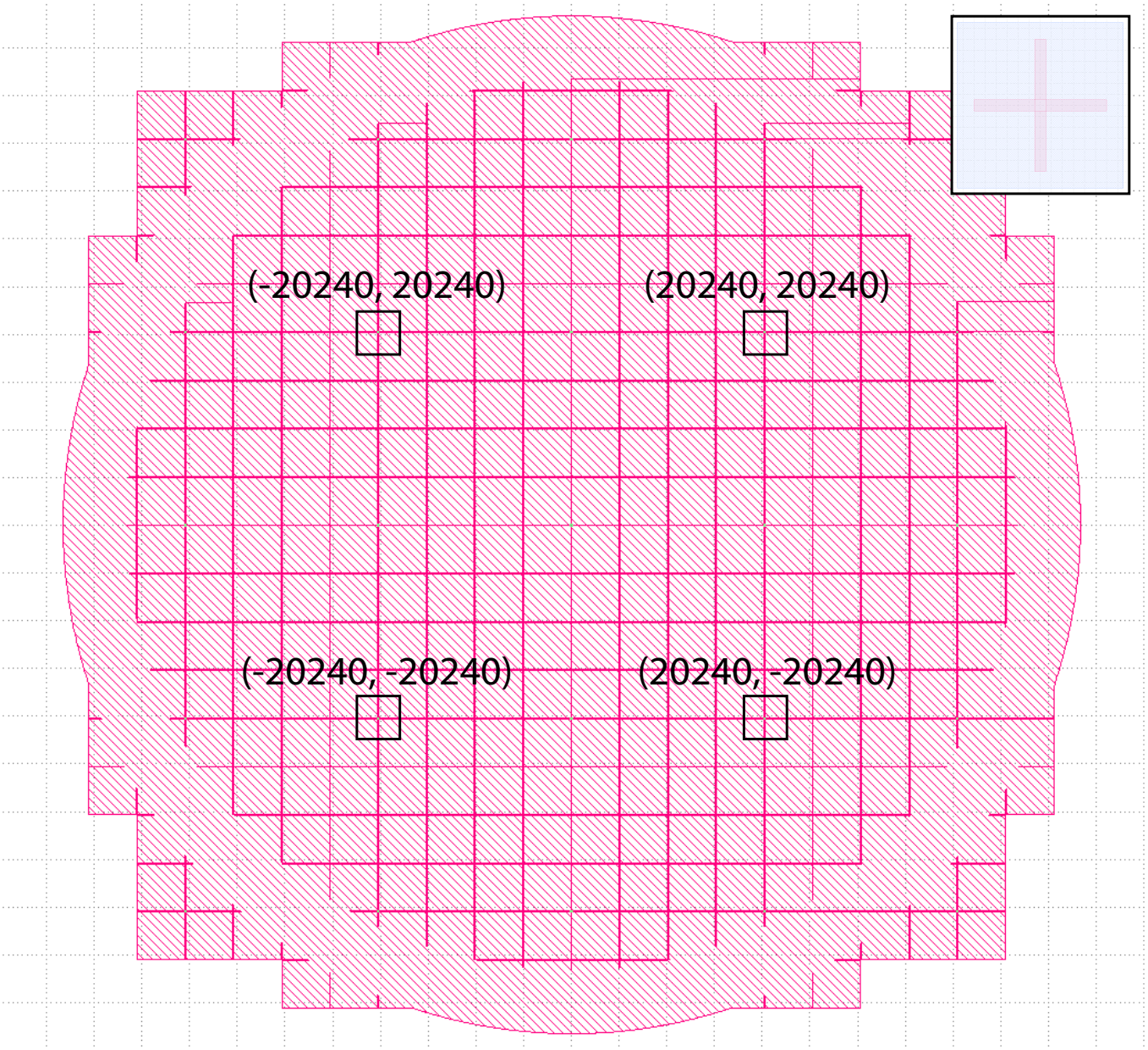

FIG. 3. Design layout to separate a 4-inch wafer into chips. Four alignment markers (cross) are used to align the chip release layer to the waveguide pattern.

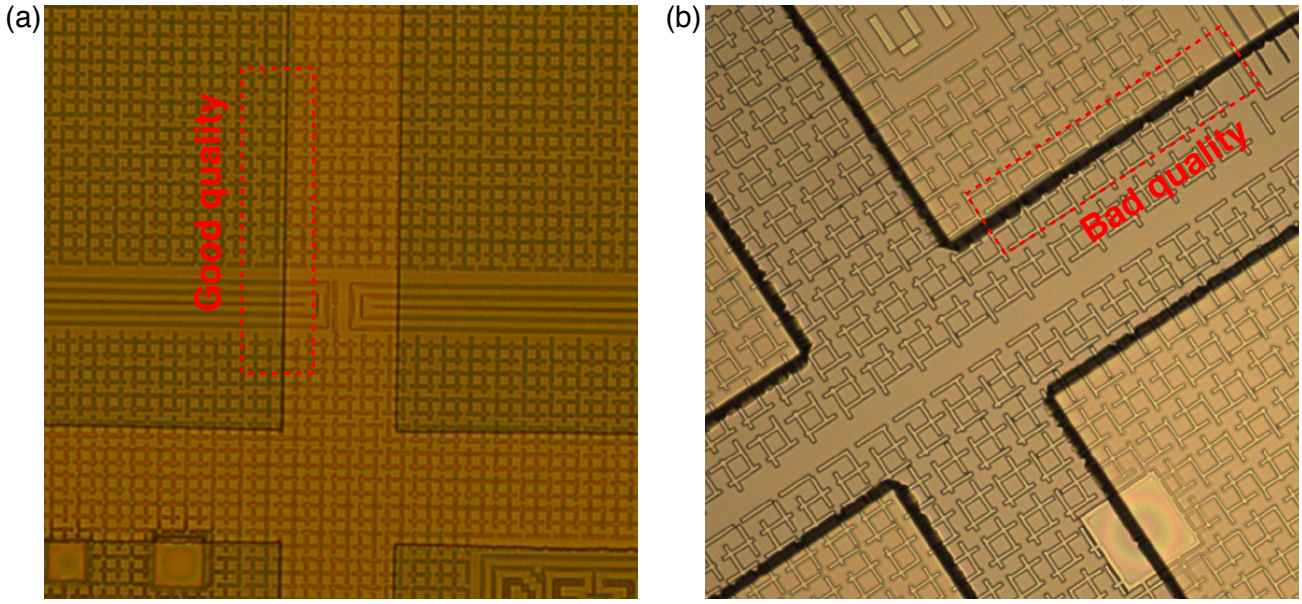

FIG. 4. Microscope images of chip boundaries after photoresist development, comparing good (a) and bad (b) lithography quality.