# Fabrication of aluminium airbridges for microwave interconnects on lithium niobate on Damascene silicon nitride photonic chips

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**Here we discuss the wafer-scale fabrication process flow of aluminium airbridges for microwave (MW) interconnects on lithium niobate on Damascene silicon nitride (LNOD) photonic chips. We also discuss the subsequent chip release procedure that preserves the bridges allowing for safe release of these delicate structures.**

Thin-film lithium niobate on insulator (LNOI) has proved to be an effective solution for transferring bulk electro-optical devices to the domain of integrated photonics. This platform has been successfully employed for realization of electro-optic frequency combs [1], quantum interfaces [2] and high-speed modulators [3]. Owing to commercial availability of LNOI wafers, the field is developing very rapidly, offering more advanced chip-scale electro-optic platforms and devices. Among those, there is an LNOD platform that combines ultralow losses of Damascene silicon nitride photonic circuits with electro-optic modulation capability of lithium niobate. This is achieved by direct wafer bonding of a lithium niobate on insulator (LNOI) wafer to Damascene silicon nitride wafer [4]. The platform has demonstrated high quality factors up to $4\times10^6$. Generation of electro-optical combs and of supercontinuum and laser diode self-injection locking were demonstrated with LNOD devices [4, 5]. So far, the applications of the platform did not require any advanced design of microwave circuitry. However, it is required to utilize an electro-optic transducer for quantum networks, for example. Complicated microwave circuitry inevitably intersects with photonic waveguides and a work-around solution is required to keep devices operational. This is achieved by introducing an air-bridge whichs allows to connect the fractions of the microwave circuitry without crossing optical waveguides [6]. Below, we focus, step by step, on how those bridges are fabricated.

## I. DEVICES DESIGN AND FABRICATION

The functions of the air bridges in the design used for the initial tests were to fix the electric potential of metal patches separated by Nb coplanar waveguide feedlines, and to enable crossings between the microwave feedlines and optical waveguides. The first application is to make sure the ground plane of the coplanar waveguide is properly defined, does not allow for magnetic flux vortices, and provide a clean environment for the microwave resonator. The second use is to make sure the optical mode does not collide with metal pieces during its propagation on the chip, as the large conductance of the metal at optical frequencies result in photon absorption that significantly reduce the guided optical power and can completely compromise the working of the device. The optical mode propagating in these LNOD waveguides (see Fig. 1a) was simulated using finite element method software (see Fig. 1b) to obtain the contribution of the different materials to the optical energy. The participation ratio of a restricted region of the simulation to the optical mode was computed as

$$\pi_{\text{material}} = \frac{\int_{\text{material}} |E_{\text{opt}}|\ d\vec{r}}{\int_{\text{total}} |E_{\text{opt}}|\ d\vec{r}}. \tag{1}$$

Keeping the participation ratio of the optical electric field in the air bridge below the one of the coplanar electrodes (see Fig. 1c) should guarantee that they do not introduce measurable optical losses, as the contribution of the electrodes themselves was deemed insignificant from previous finite element simulation for the considered gap.

There are two kinds of airbridges that are required for the MW circuitry operation: 1) connecting signal lines segments ("small" bridges), and 2) connecting ground electrodes segments ("large" bridges). The both types has the same structural components: pillars and an arch. The bridges of the first class have got the following dimensions for the pillars and the arch respectively: $10\times10$ $\mu$m$^2$ and $25\times10$ $\mu$m$^2$. The same parameters for the second class are the following: $25\times10$ $\mu$m$^2$ and $25\times55$ $\mu$m$^2$.

The bridges are manufactured on an LNOD wafer where lithium niobate ($LiNbO_3$) tapers and niobium (Nb) electrodes have been already fabricated. The first step is spin-coating of photoresist for a photolithography step that opens pillars areas for contact with the Nb electrodes. The resist used is 2-$\mu$m-thick ECI 3027 (on Süss ACS200 GEN3 automatic coater). After exposure on a direct laser writer (Heidelberg Instruments MLA150) and development, the resist is reflown on a hot plate with temperature of 140 °C (EPFL CMi Z07). The wafer stacks illustrating these steps and the associated optical micrographs are given on Fig. 2. This step results in the characteristic rounded profile of the bridge arch. After refow, the bridges shape is characterized on a mechanical profilometer (Bruker Dektak XT) to check the expected height of the bridge (cf. Fig. 3).

The entire wafer is then covered by a 500-nm-thick layer of aluminium (Al) in an e-beam evaporator (Plassys

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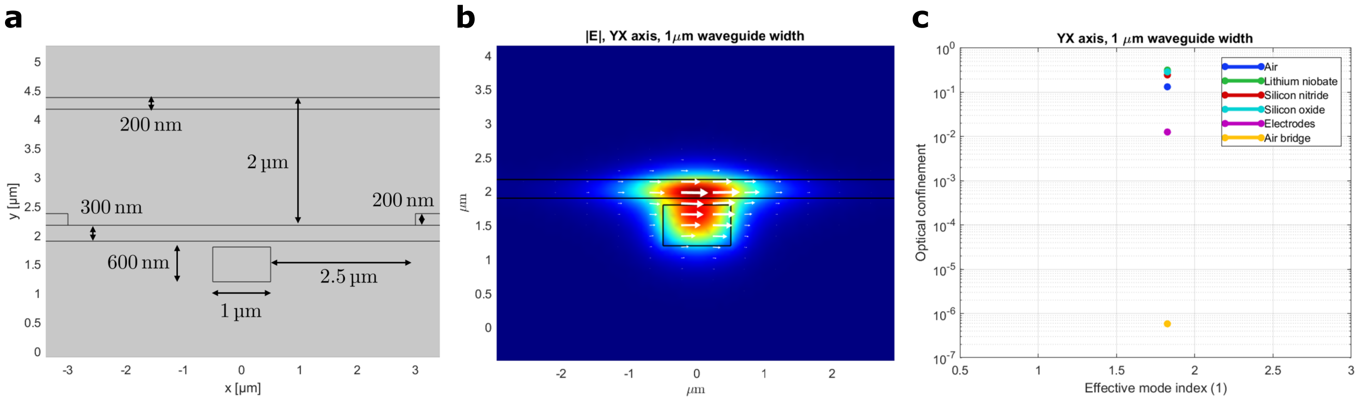


Figure 1. **Simulation of metal-induced optical loss**. (a) Schematic cross-section of an LNOD waveguide with an airbridge with annotations of the critical dimensions. (b) TE optical mode propagating in the LNOD waveguide at 1550 nm obtained by finite element simulation. (c) Participation ratio of the electric field in the different materials of the simulation window. The marginal contribution of the airbridge indicates that no increase of optical loss should be induced by the air bridge for these dimensions.

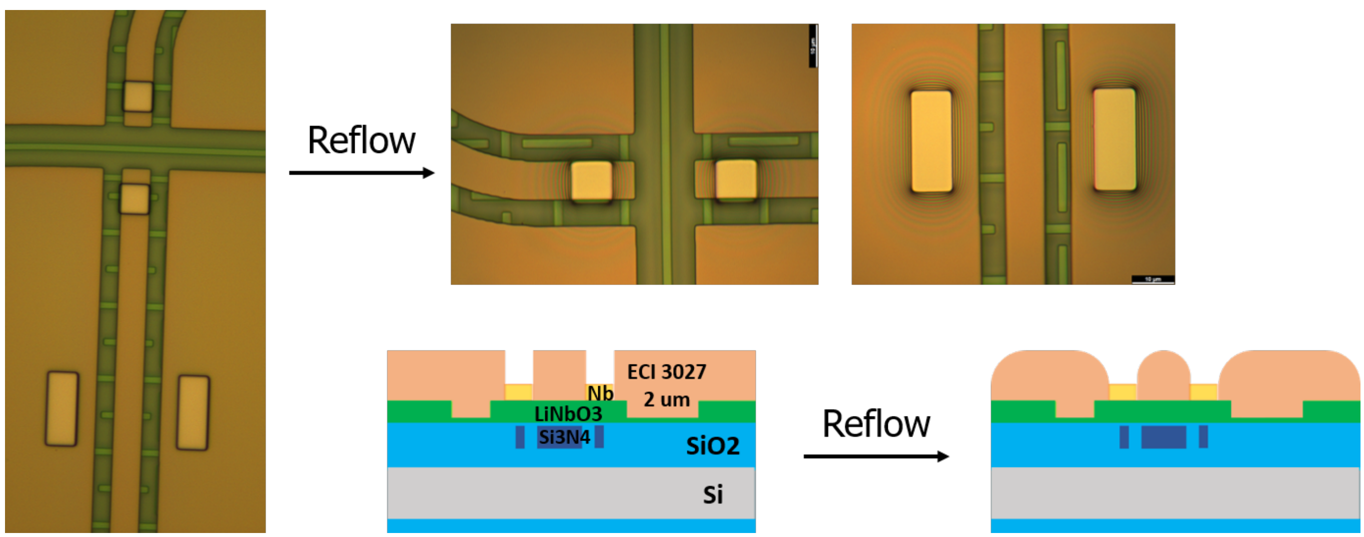


Figure 2. **Pillars areas opening**. Optical micrographs (top row) and wafer layer stacks (bottom row) illustrating pillars patterning of the bridges.

MEB550SL3 UHV Evaporator), see Fig. 4. Before evaporation, a wafer is exposed to ion beam for 8 min that is used to remove native oxide from the opened pillars areas enabling better contact between an Al bridge and a Nb electrode. After evaporation, a wafer is oxidized in a dedicated chamber. We oxidize the surface of aluminum film using oxygen of high purity inside the vacuumed chamber to avoid its reaction with ambient oxygen outside the chamber.

To pattern bridges arches, another photolithography step is required. This is done with 1.5-$\mu$m-thick ECI 3007. The photoresist is spin-coated in the ACS200 automatic-coater, with a soft-bake at 100°C. After exposure with the maskless laser-writer (Heidelberg Instruments MLA150), development is done in the ACS200 with a post-exposure bake at 110°C. This second photolithography only keeps photoresist on top of the future arches (see Fig. 5). Optical micrographs indicate corrugated shape of the areas protected by the resist. This requires further investigation at higher magnification, and one can use a scanning electron microscope (Zeiss MERLIN) to accomplish that (see Fig. 6). SEM characterization reveals that, although photoresist is slightly overdeveloped on the top, it still covers the whole area of the pillar on the bottom. Al is removed by wet etching (Plade Metal wetbench) in $H_3PO_4$ 85% + $CH_3COOH$ 100% + $HNO_3$ 70% at 35 °C for 3 minutes (see Fig. 7).

Next, the resist covering the bridges arches and lying beneath them is to be removed. This is accomplished by putting the wafer in the Remover 1165 baths (UFT Resist wetbench) at 70 °C for 20 minutes (10 minutes is spent in each of the two baths). After that, a wafer goes through FTT and TT water baths for rinsing and SRD machine for drying (see Fig. 8).

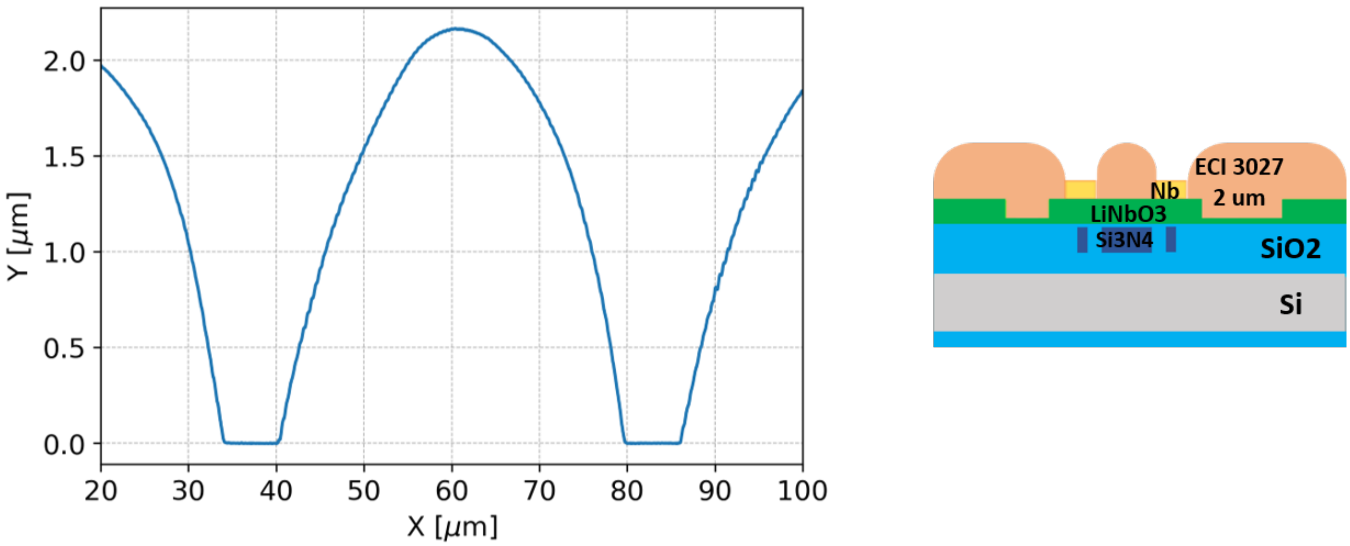


Figure 3. **Bridge profile after reflow**. (Left) Mechanical profilometry data of a "large" bridge from wafer D91_01. (Right) A wafer layer stack diagram illustrating the concerned processing step.

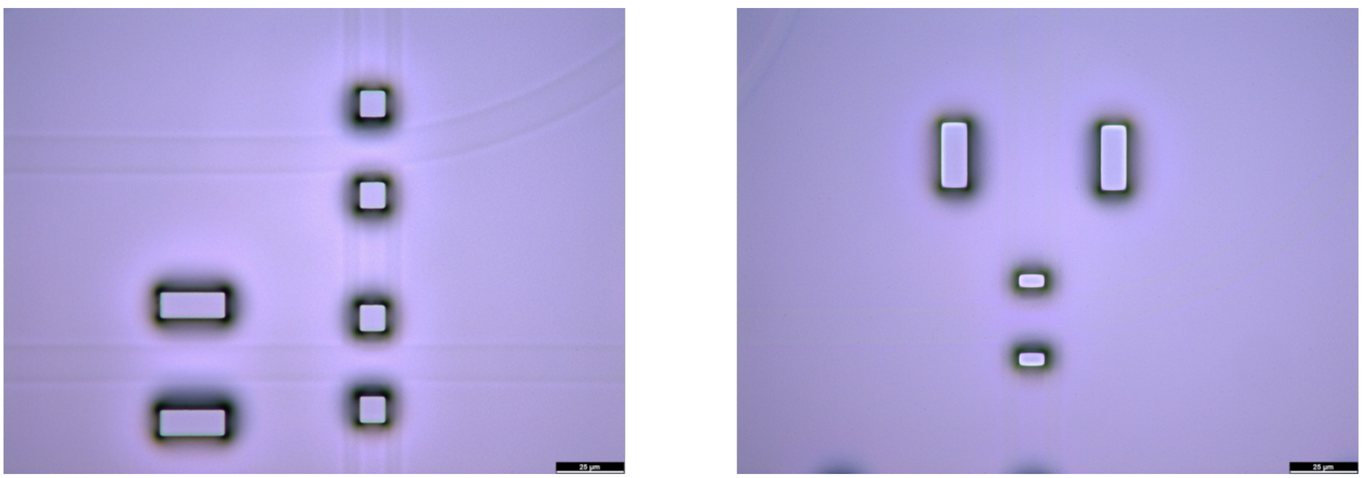

Figure 4. **Aluminium evaporation**. Optical micrographs of an LNOD wafer after deposition of 500 nm of Al.

Now that the bridges are fabricated, the wafer has to be separated into chips. Chip release starts with photolithography on a mask aligner (Süss MA6Gen3) with a 10-$\mu$m-thick negative resist layer (AZ 15nXT). Prior to photoresist spin-coating, wafer surface is subject to dehydration at 125 °C for 5 minutes as well as HMDS monolayer deposition to ensure good adhesion both on $LiNbO_3$ and Nb. Although the air bridges are exposed to surface tension force during spin-coating, they survive this step (see Fig. 9). After development, exposed areas (dose of 320 mJ$\cdot$cm$^{-2}$), as the resist is negative, are kept on the wafer, protecting areas of prosprective chips, separated with 100-$\mu$m-wide gaps (see Fig. 10). Next, the wafer is etched in a fluorine-based chemistry dielectric plasma etcher (SPTS APS) for 15 minutes by in a mixture of $C_4F_8/H_2$/He (see Fig. 11). During this etching step 4 $\mu$m of $SiO_2$ is etched as well as thin $LiNbO_3$ slab ($<$ 50 nm). After etching, the wafer is inspected on transparent film interferometric setup (Filmetrics F54) to check if there is any oxide left. The reflectance spectrum is expected to exhibit no oscillations and is to be given by the monotonic decay of intensity with an increase in wavelength. This is an indication that there is no oxide left. Deep $SiO_2$ etching is then followed by deep Si etching (Bosch process [7], DRIE recipe, 320 cycles) in a deep reactive ion (DRIE) etching tool (SPTS Rapier). After that, etched trenches depth is inspected on an optical microscope by, first, focusing on the wafer top surface and, second, focusing on the bottom of the trench (see Fig. 12). Then, the coordinates of a microscope objective in these two positions are substracted, yielding, for the wafer whose processing history is discussed here (D91_01), 262 $\mu$m of etched depth into the wafer Si carrier. Provided that the wafer has got the thickness of

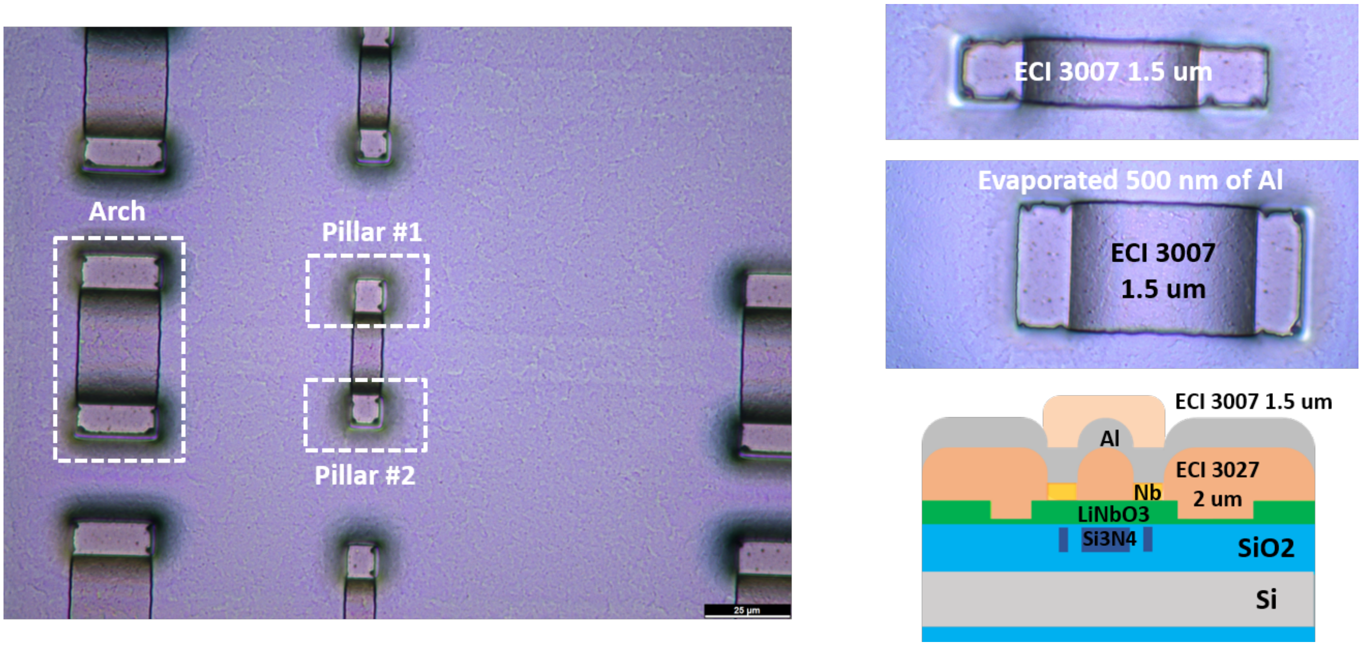


Figure 5. **Aluminium etching photolithography**. (Left) An optical micrograph of a "large" and "small" bridges. (Right, top) Optical micrographs of the bridges at higher magnification. (Right, bottom) A wafer layer stack diagram illustrating the concerned processing step.

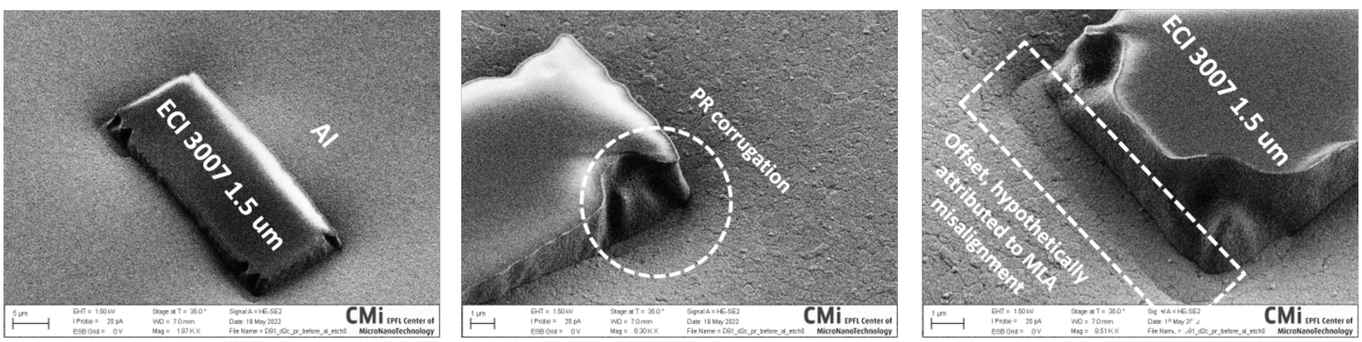


Figure 6. **SEM of aluminium etching photolithography**. Corrugated shape of the protected areas - observed in the optical microscope - reveals itself as over-developed parts of the resist what could be hypothetically attributed to over-exposure induced by extra light reflections from Al covering the surrounding rounded topography.

535 $\mu$m, for proper chips separation, mechanical grinding should reduce the thickness down to 245 $\mu$m. For mechanical grinding (DAG810), the wafer is attached to tape on Powatec Wafer Mounter P-200 (the top is attached to the tape). Once grinding is done, the taped wafer goes through the ultra-violet curing tool (U-200, speed "0", 7 passes), and the obtained chips are picked up manually by a tweezer (see Fig. 13).

As it may be evident from the previous steps description, the chip release resist is not removed before mechanical grinding. And, it is this resist layer that is in direct contact with the tape. This is done with an intension to protect air bridges during mechanical grinding and tape cure and separation. However, this effective protective measure is taken at expense of more tedious chip-scale photoresist stripping than that of the wafer-scale test. Still, stripping is cleanly done in an oxygen plasma reactor (Tepla GiGAbatch) using 20-minutes-long high-power recipe (600 W). This procedure (see Fig. 14) proves to be safe (see Fig. 15) for the air bridges resulting in the yield of 100% on characterized samples. After resist stripping, the bridges are again characterized on a mechanical profilometer to verify if there are any changes of their height. The results suggest that instead of expected 2 $\mu$m, actually measured values are 3 $\mu$m for the "small" bridges, and 5.5 $\mu$m for the "large" bridges (see Fig. 16). This dramatic change of the bridges height may be hypothetically attributed to an impact of surface tension forces. These forces may deform the initial shape of the bridges, changing arches curvature, when the wafer

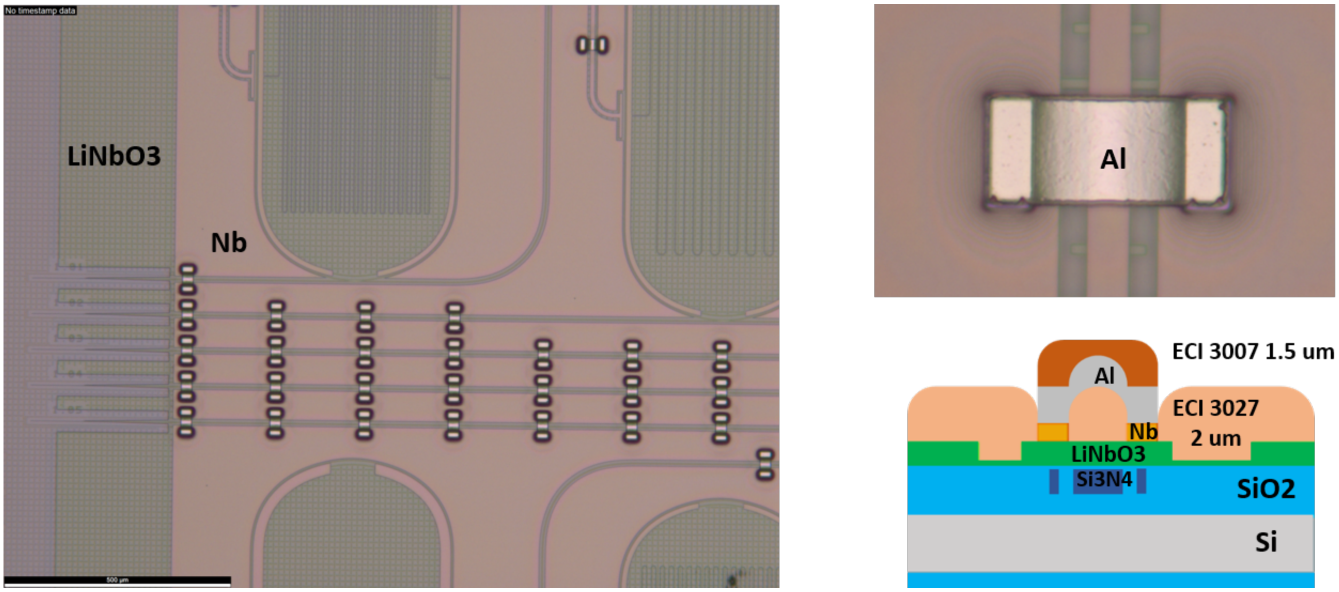


Figure 7. **Aluminium wet etching**. (Left and top right) Optical micrographs of an LNOD wafer fragment and of a "large" airbridge after Al wet etching. (Bottom right) A wafer layer stack diagram illustrating the concerned processing step.

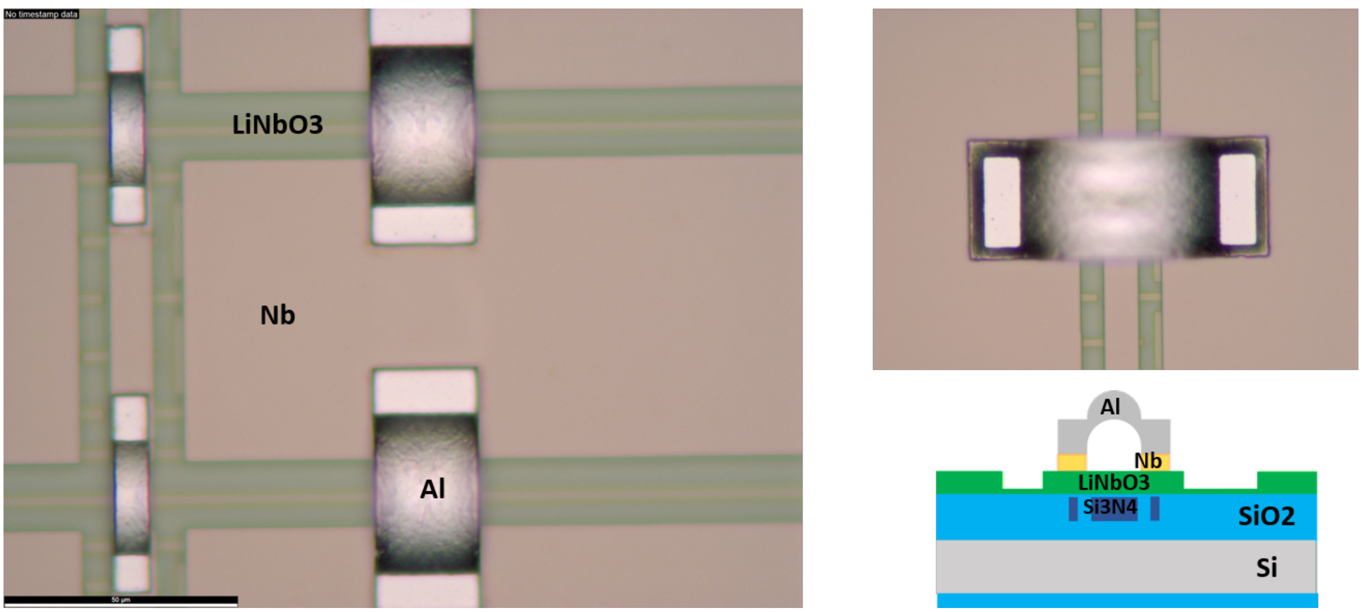


Figure 8. **Photoresist removal.** (Left and top right) Optical micrographs of an LNOD wafer fragment and of a "large" airbridge after photoresist stripping. (Bottom right) A wafer layer stack diagram illustrating the concerned processing step.

passes through the steps of resist spin-coating and stripping. The bridges are then tested on an electrical probe station (MPI TS150 Prober Station) to check if there is any current passing through a bridge once voltage is supplied to two ground electrodes segments. The results of these test are given on Fig. 17.

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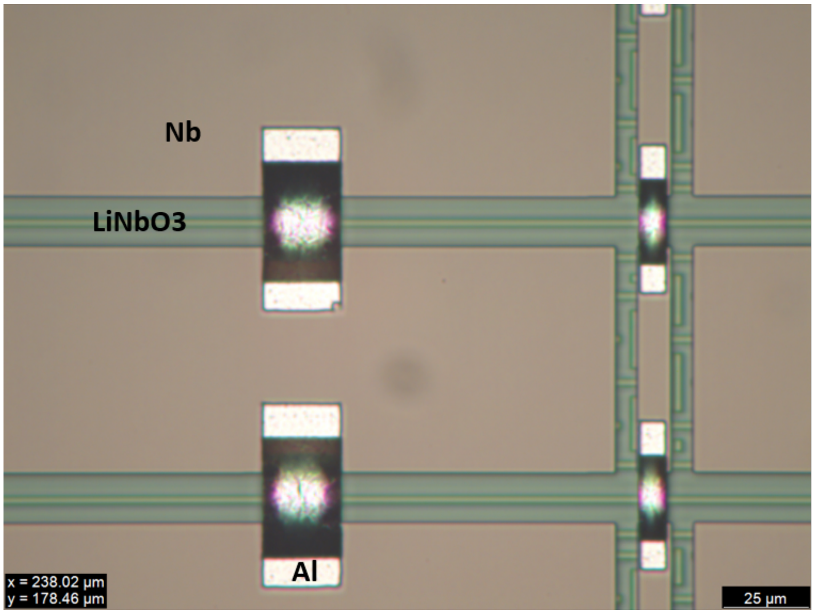


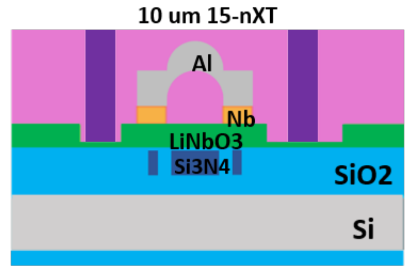
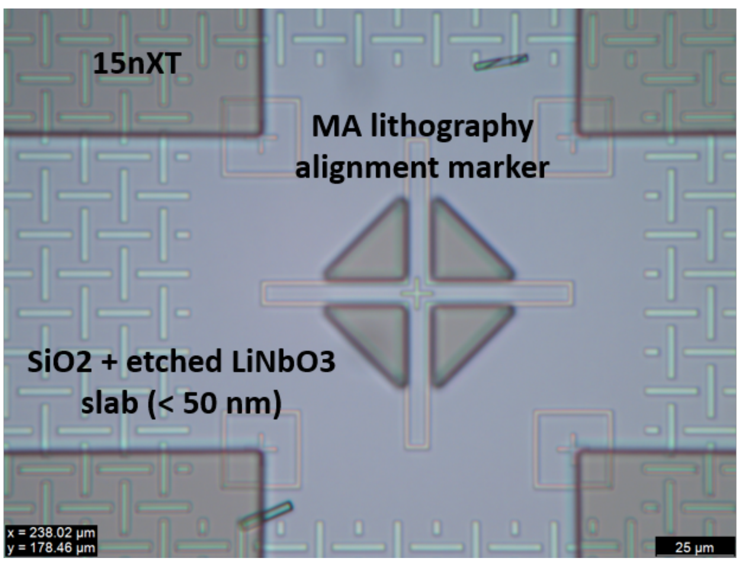




Figure 9. **Chip release spin-coating**. (Left) Optical micrograph of the wafer after coating (Right) A wafer layer stack diagram illustrating the concerned processing step.



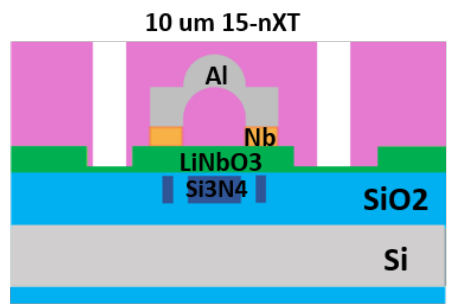




Figure 10. **Chip release photolithography**. (Left) Optical micrograph of the wafer after chip release resist pattern development (Right) A wafer layer stack diagram illustrating the concerned processing step.

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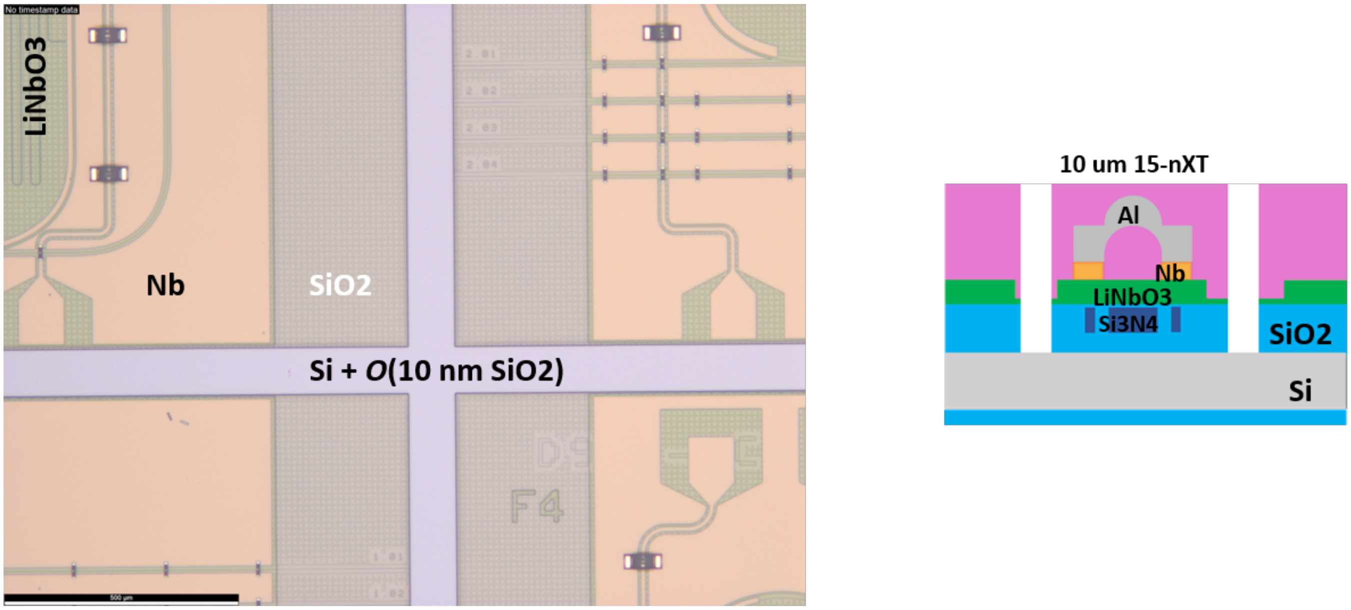


Figure 11. **Deep $SiO_2$ etching**. (Left) Optical micrograph of the wafer after deep oxide etching in fluorine-based-chemistry plasma dielectric etcher. (Right) A wafer layer stack diagram illustrating the concerned processing step.

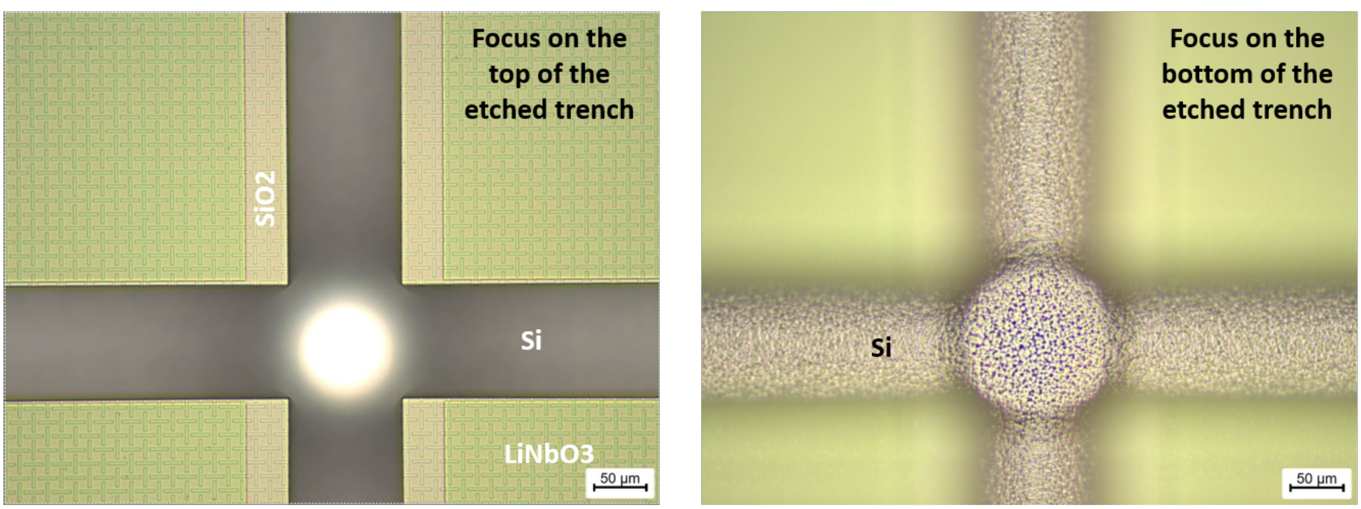


Figure 12. **Deep Si etching**. (Left) Optical micrograph of the wafer after deep silicon etching with the focus on the wafer top surface. (Right) Optical micrograph of the wafer after deep silicon etching with the focus on the etched trench bottom.

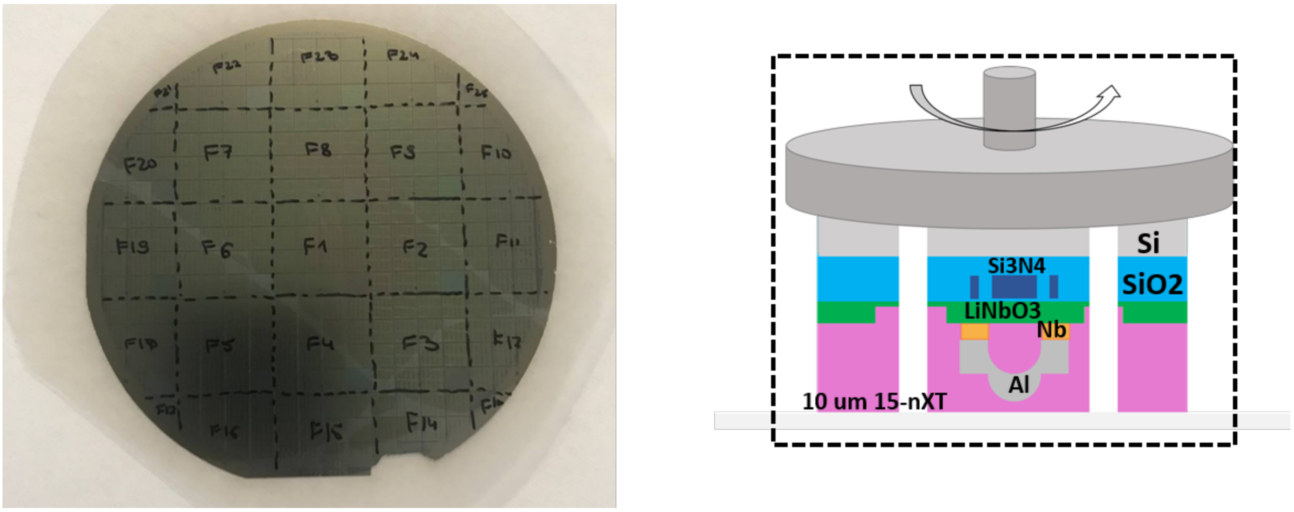


Figure 13. **Wafer backside mechanical grinding**. (Left) Photo of a grinded wafer after UV-curing with the wafer fields demarcation for more conveninet manual chip release. (Right) A wafer layer stack diagram illustrating the concerned processing step.

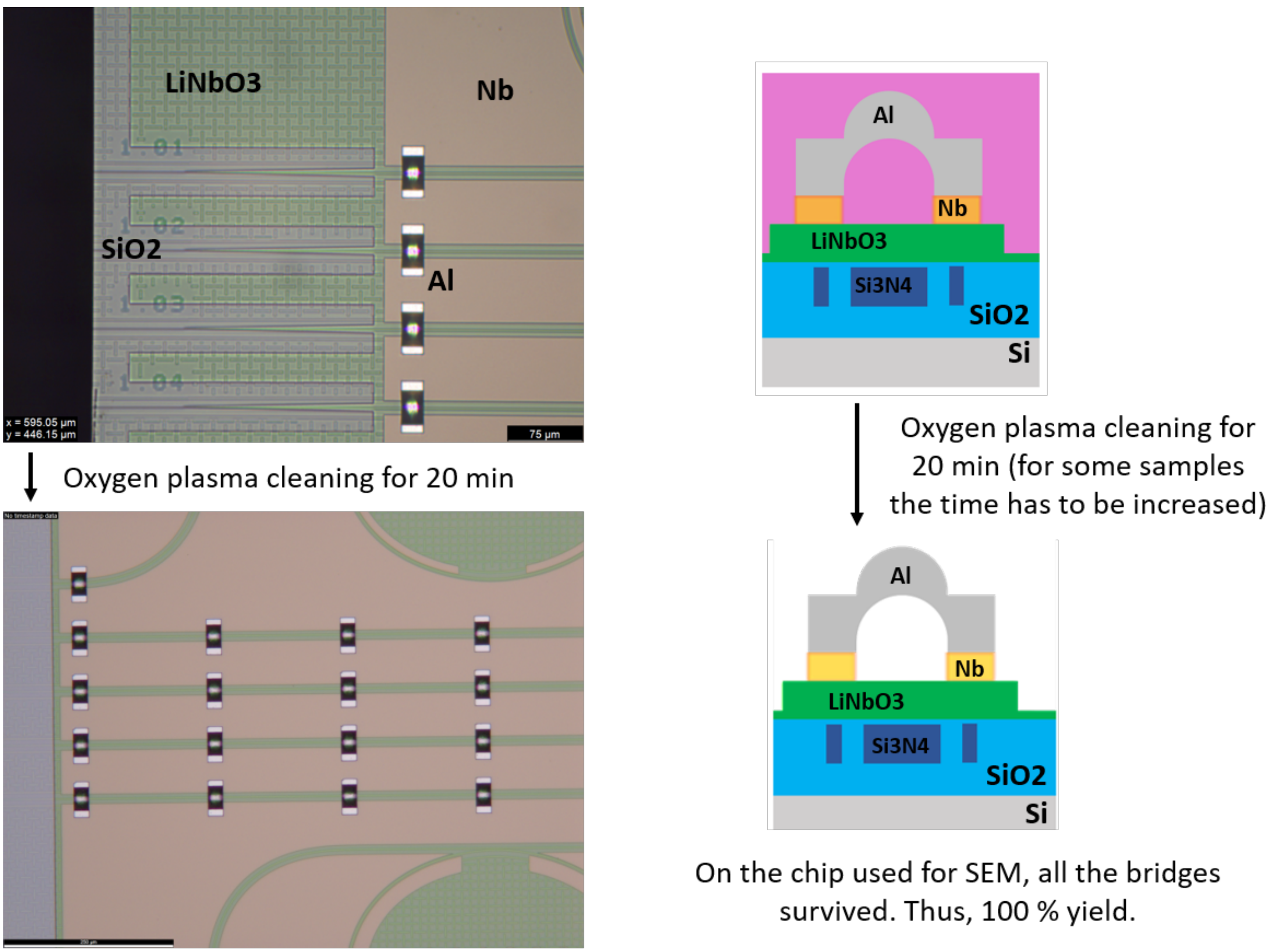


Figure 14. **Photoresist stripping**. (Top) Optical micrograph and a chip stack diagram for a chip right after it was separated from the cured tape. (Bottom) Optical micrograph and a chip stack diagram for a chip after photoresist removal in an oxygen plasma asher.

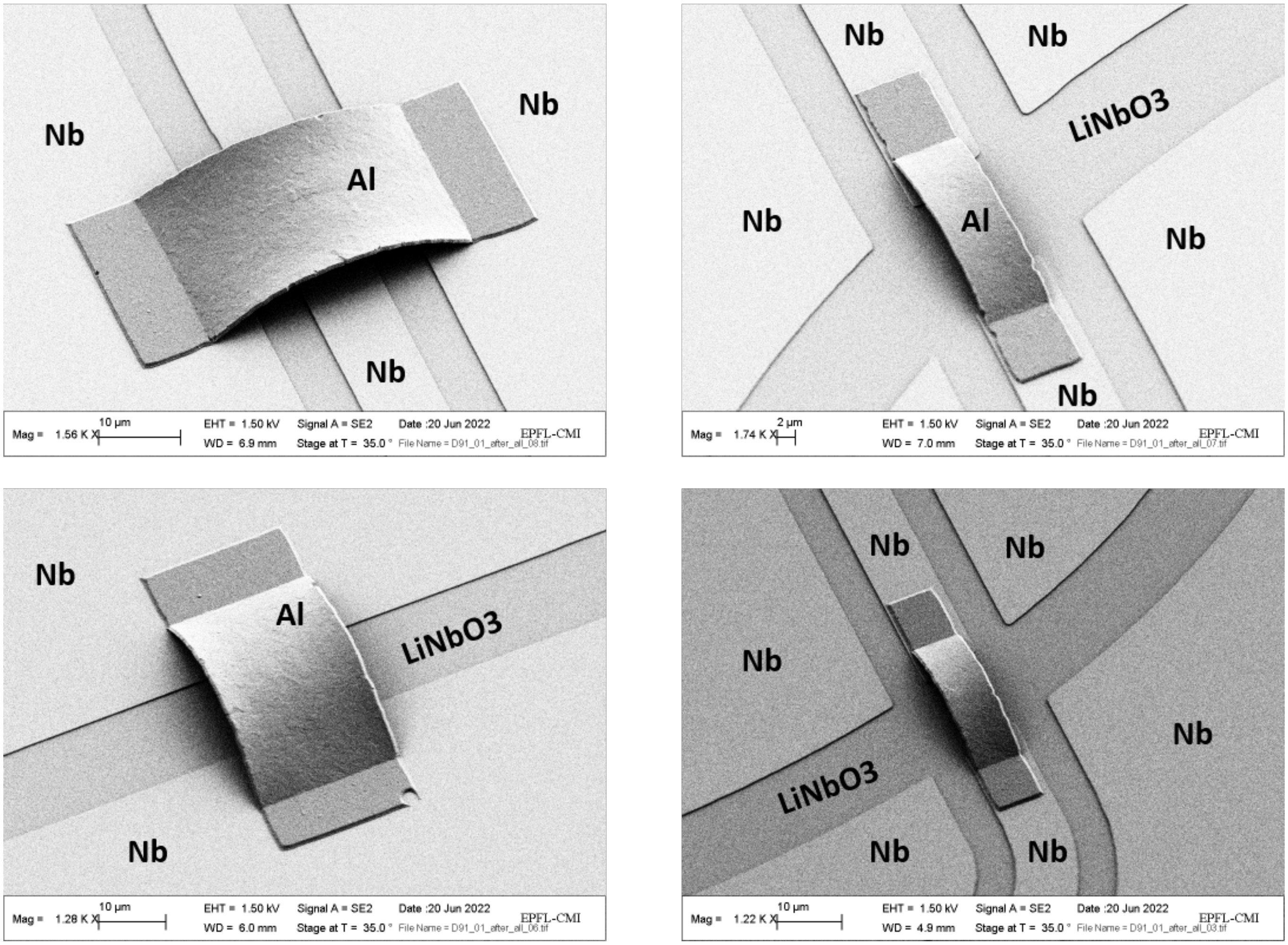


Figure 15. **Released air bridges SEM characterization**. SEM images showing air bridges condition after photoresist removal. These devices are now ready for cryogenic quantum electro-optical transduction experiments.

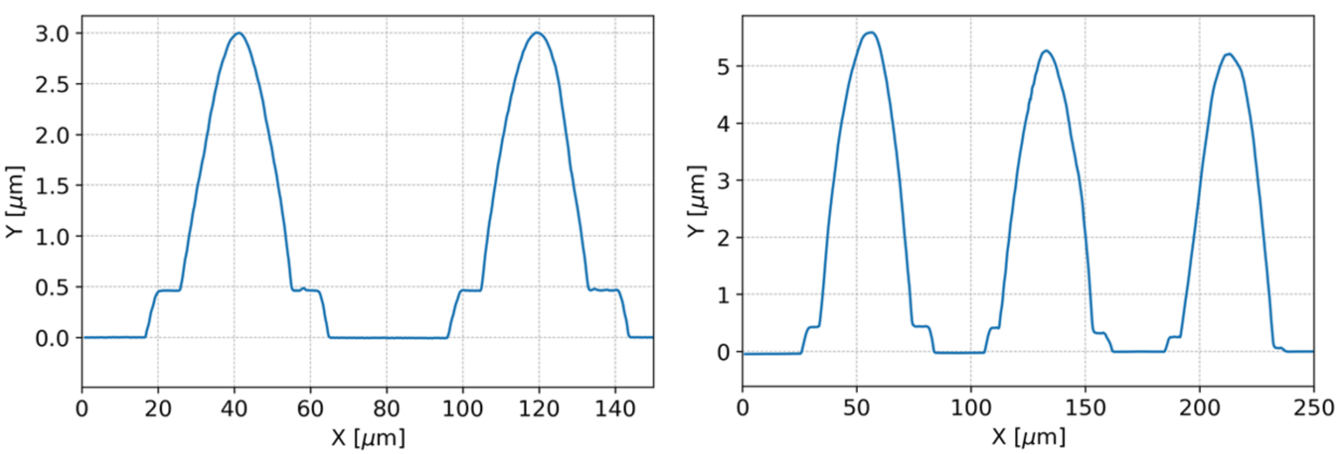


Figure 16. **Released air bridges mechanical profilometry characterization**. Mechanical profilometry scans of two "small" air bridges (left) and three "large" airbridges (right).

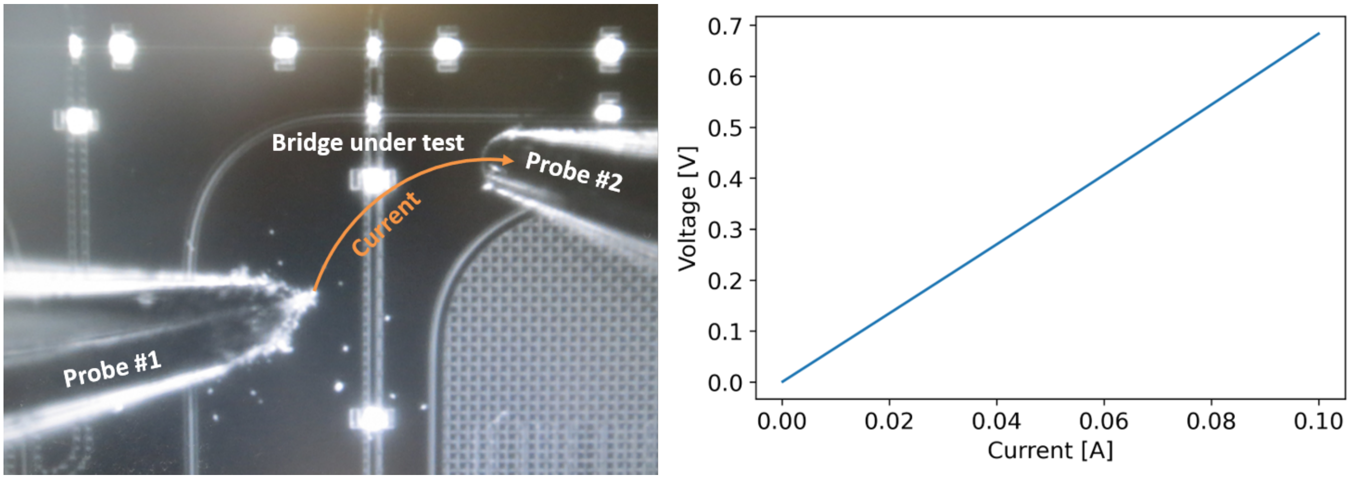


Figure 17. **(Left)** Optical micrograph of the experiment to test the air bridges interconnects. **(Right)** UI-curve collected from the bridge junction depicted on the left.