High aspect ratio Si_3N_4 nanomembranes

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A fabrication method for large-area, high-stress LPCVD Si_3N_4 membranes is presented. These devices can be used as mechanical resonators with very low dissipation, exploiting dissipation dilution. A phononic crystal pattern allows to work with a high-order localized mode, shielded from acoustic radiation in the substrate. The procedure is amenable to most research clean rooms, requiring conventional lithography techniques and wet etching in KOH for device undercut.

Keywords: Si_3N_4, MEMS, mechanical resonator, pressure sensor, high stress, KOH, wet etch

FABRICATION PROCESS

Patterned and unpatterned membrane samples are fabricated on the same 100 mm wafer. Stoichiometric, high stress Si_3N_4 is grown by low pressure chemical vapor deposition (LPCVD) on both sides of a 200 µm-thick silicon wafer. The initial deposition stress is estimated a posteriori from the observation of membrane resonant frequencies, and varies in the range 900-1100 MPa, changing slightly with deposition run.

The fabrication process relies on bulk wet etching of silicon in KOH through the whole wafer thickness, to create openings for optical access to the membranes samples [1–4]. The extremely high selectivity of Si_3N_4 to Si during KOH etching allows the use of the backside nitride layer as a mask, to define the outline of the membranes on the frontside.

Initially, the frontside nitride (Si_3N_4) layer is patterned with h-line photolithography and CHF_3/SF_6-based reactive ion etching (RIE) (steps 2-3 of figure 1). The photoresist film is then stripped with a sequence of hot N-Methyl-2-pyrrolidone (NMP) and O_2 plasma; this procedure is carefully repeated after each etching step. The frontside nitride layer is then protected by spinning a thick layer of negative-tone photoresist (MicroChemicals AZ®15nXT), prior to flipping the wafer and beginning the patterning of membrane windows on the backside nitride layer (steps 4-5). We noticed a reduction in the occurrence of local defects and increased overall membrane yield when the unreleased membranes on the frontside were protected from contact with hot plates, spin-coaters and plasma etchers chucks. The backside layer is then patterned with membrane windows, in a completely analogous way. The exposure step requires a wafer thickness-dependent rescaling of membrane windows, to account for the slope of slow-etching planes in KOH, and careful alignment with frontside features.

After stripping the photoresist, the wafer is installed in a PTFE holder for the first wet etching step in KOH at $\approx 75\,^{\circ}C$ (step 6). The holder clamps the wafer along its rim, sealing off the wafer frontside with a rubber O-ring, while exposing the backside to chemical etching by KOH. This procedure is necessary to ensure that PnC membranes are suspended correctly: we noticed that releasing PnC samples by etching from both sides of the wafer produced a large number of defects in the phononic crystal, probably due to the particular dynamics of undercut and stress relaxation in the film. The wafer is etched until 30-40 µm of silicon remains, leaving the samples robust during the subsequent fabrication steps. The wafer is then removed from the KOH bath and the PTFE holder, rinsed and cleaned in concentrated HCl at room temperature for 2 hours [5].

Subsequently, the wafer is coated with thick, protective photoresist and diced into $8.75\,\text{mm} \times 8.75\,\text{mm}$ chips, and the remainder of the process is carried on chip-wise. Chips are cleaned again with hot solvents and O_2 plasma, and the membrane release is completed by exposing chips to KOH from both sides (step 7). The temperature of the solution is lowered ($\approx 55 - 60\,^{\circ}C$), to mitigate the perturbation of fragile samples by buoyant N_2 bubbles, a byproduct of the etching reaction. After the undercut is complete, the samples are carefully rinsed, cleaned in HCl, transferred to an ethanol bath and gently dried in a critical point dryer (CPD).

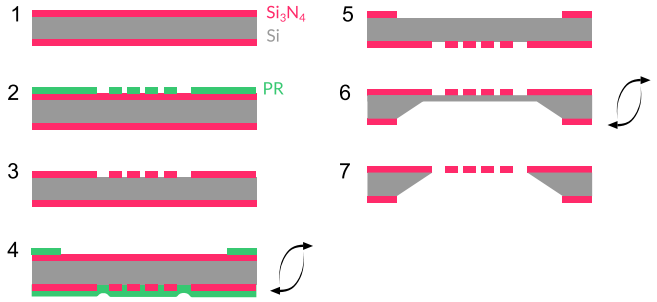

FIG. 1. Main steps of the fabrication process. Magenta - Si_3N_4; gray - Si; green - photoresist.

DETAILED INSTRUCTIONS AND PITFALLS

- **Lithography.** Etch a sufficient number of alignment markers on the frontside to guarantee an acceptable alignment on the backside. 4-6 should be sufficient for a 100 mm wafer. Remember to flip the

mask according to the settings used by the selected exposure tool.

- **Post-etch cleaning.** Make sure to strip thoroughly the resist after etching. What works best is a sequence of 30 s / 1 minute O2 plasma at high power to etch the hardened crust - 10 min in NMP at 70 °C to strip the bulk of the photoresist, and O2 plasma at high power for 3 / 5 minutes to clear off the residues from the bath. Monitor the dimensional accuracy of features and the amount of contamination with SEM, at least after the frontside etching step.

- **Wet etching.** The best practice is to clean beakers and holders with IPA and fiberless cloths prior to the process. Regulate the concentration of KOH with a densimeter at room temperature, then heat to desired temperature and wait for the hotplate to stabilize; the temperature will overshoot significantly then drop down when the holder is inserted. Start timing when you see tiny N2 bubbles being produced at the exposed Si surfaces (1-2 minutes delay). Use a stirrer to slowly agitate the KOH bath.

  When etching PnC samples mount in frontside-protecting holder (Fig. 2); make sure that the wafer flat is aligned with the corresponding feature on the holder because the tolerances are quite tight and the wafer can easily get stuck in a tilted configuration and will be difficult to remove without breaking. If PnC samples are etched from both sides, samples will break dramatically because of the anisotropic etch and stress relaxation dynamics (as in Fig. 3). Instead, splitting the process in two steps works very well: the first etch from the backside only should leave 30-50 um of silicon (etched depth can be measured with an optical microscope with a high magnification objective and a large aperture; the displacement of the stage between the positions where the surface and the bottom of the pit are in focus provides a good estimate of the etched depth), and the chip-wise, double-sided etch provides the advantage that particles from the dicing process can be cleared off and one does not need to separate manually the samples.

  Rinse abundantly, especially when using a chip holder which constrains the flow in the orthogonal direction. One technique which works well is slowly moving up and down the chip holder, crossing the interface of the DI water bath 5-10 times. Repeat a few times, each time in a fresh DI water bath. Make sure that the pH of the water bath and in the holder blind holes is 'adequately neutral' (pH $\approx 5.5 - 8.5$), both after KOH etch and HCl cleaning.

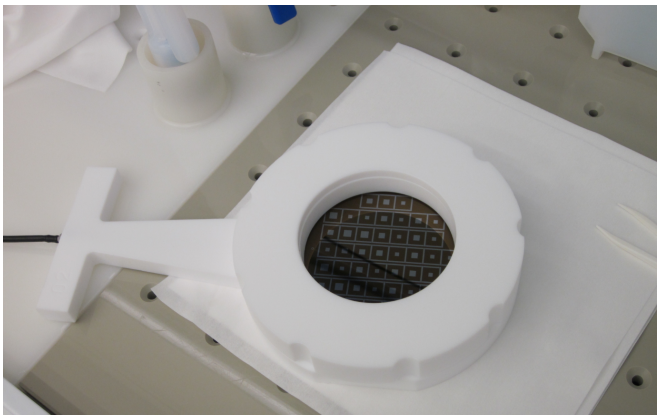

FIG. 2. A wafer is mounted in the mechanically-sealing PTFE holder. The backside with membrane windows will be exposed for KOH etch.

- **Critical Point Drying.** The more delicate the samples, the gentler the transfers should be, in terms of mounting conditions, steadiness of movements, control of bath perturbations and all factors that can influence sample survival. Trampolines and strings are much more fragile than PnC and unpatterned membranes, for a given aspect ratio.

  Note that CPD is not strictly required in terms of stiction failure, for completely released membrane samples, but is still useful: if done properly, it can be gentler and cleaner than manual drying. Make sure the samples are immersed sufficiently long in ethanol to have a good exchange of liquid in the proximity of the chips.

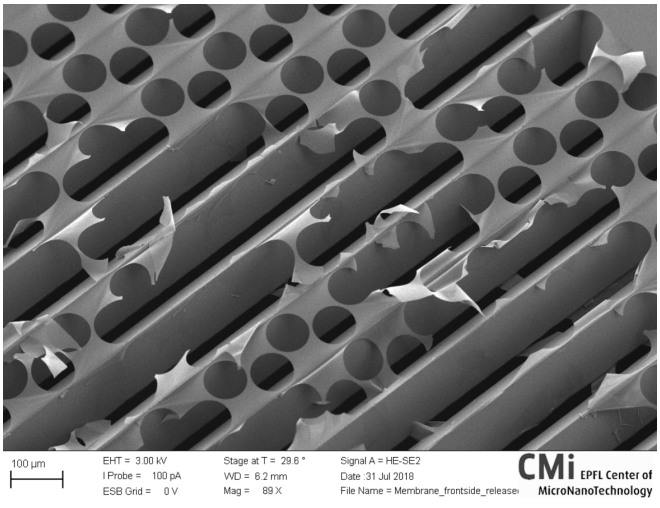

FIG. 3. A PnC sample after partial double-sided undercut. Triangular prisms of silicon following [111] crystallographic directions are obtained as a result of anisotropic KOH etch.

FURTHER READING

- The devices described here are employed for the experiments in [6].
- Very similar samples and fabrication methods were previously reported in [1–4].
- Detailed fabrication methods and insight to suspend extremely large-areas Si_3N_4 membranes are reported in [7]. In that context, the devices were meant for use as transparent pellicles for EUV lithography.

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